DEVELOPMENT OF TEMPERATURE-STABLE, SOLDERABLE PVD REAR METALLIZATION FOR INDUSTRIAL SILICON SOLAR CELLS

Julia Kumm, Hassan Samadi, Philip Hartmann, Sebastian Nold, Andreas Wolf, Winfried Wolke
Fraunhofer Institute for Solar Energy Systems ISE
Heidenhofstrasse 2, D-79110 Freiburg, Germany, julia.kumm@ise.fraunhofer.de

ABSTRACT: In this work a solderable and temperature-stable rear metallization based on physical vapour deposition (PVD) is developed. A common Al metallization is complemented by a solder stack that consists of a sputter deposited TiN barrier layer and a thin solderable top layer, which are deposited on an industrial PVD machine in one process sequence. Peel-tests confirm sufficient adhesion for conventionally soldered cell interconnectors even when annealing at 425°C for 18 minutes before soldering, as well as stability of the solder joint during thermal aging at 130°C for 85 h. Our results suggest that our Al based PVD metallization scheme is industrially-feasible, compatible with a common soldering and interconnection process, potentially cost-efficient and therefore suitable for industrial PERC and other silicon solar cells.
Keywords: Silicon solar cells, PVD, aluminum, evaporation, soldering, rear metallization

1 INTRODUCTION

Physical vapour deposition (PVD) enables metallization of PERC and other silicon solar cells, showing high efficiencies in research [1]. PVD Al forms an ohmic contact with low contact resistance to p-doped as well as to moderately doped n-type silicon which qualifies it for a wide range of solar cell applications. Additionally, thin layers can be deposited, as demonstrated for industrial PERC cells [2, 3] which reduces material, especially Ag consumption and makes PVD metallization potentially cost-efficient compared to scree-printing. However, PVD metallization has not yet been industrially implemented in large scale. One vital reason for this is the lack of solderability of a PVD Al layer, since an industrial application requires a reliable interconnection concept which enables module integration of the cells. Hereby, a concept which bases on well-established soldering of cell interconnectors is favoured. Previous approaches [4, 5] with the aim of enabling interconnection of cells with PVD Al metallization, require the introduction of new interconnection technologies. Alternatively, conventional soldering of the metallization after deposition can be enabled by adding a solderable and well-adhering PVD layer onto the PVD Al as demonstrated in [6, 7]. However, its solderability is not preserved when the metallization stack undergoes a common annealing step. Hence, as most solar cell concepts benefit from a final annealing step, practical applicability of this approach is limited. Therefore, it is desirable and the aim of this work to develop a PVD metallization which is not just initially solderable but also temperature and aging stable, and thus enables long term stable solderablilty of cells with PVD metallization after common annealing steps.

2 METALLIZATION CONCEPT

Possible applications of a temperature stable, solderable Al based PVD metallization scheme on solar cells are numerous – for the investigations in this work Passivated Emitter and Rear (PERC) silicon solar cells with evaporated Al rear metallization and LFCs in the TOPAS design [8, 9] are chosen as reference to define the demands made on the metallization scheme.

To achieve a solderable metallization scheme we complement PVD Al with a sputter deposited solder stack.

This is what our approach has in common with the investigation of Lehr et al. [7] who enable solderability of fully-processed cells by subsequently adding a solderable stack; demands at thermal stability thereby are kept low. Samadi et al. [10] additionally address challenges that arise when LFC are used.

In this work all PVD layers – evaporated Al and the sputter deposited solder stack – are deposited in one process sequence as it would for economic reasons favourably be realized in an industrial production line. This implies for LFC-PERC type cells, that the complete metallization stack is laser-fired and undergoes a forming gas anneal at 350°C before soldering and module assembly. A good thermal stability of the metallization stack is therefore crucial. To realize this, the PVD solder stack that complements the PVD Al layer should comprise a solderable top layer and a barrier layer which effectively separates the solderable layer and the Al layer. Various materials are known to be suitable barriers, we choose TiN for our investigations for its physical properties, availability and cost. We therefore suggest a structure as presented in Fig 1. The developed solder stack comprises a TiN barrier, an Ag layer as solderable topping and a thin Ti layer which is added between Ag and TiN to improve adhesion between the two materials [11].

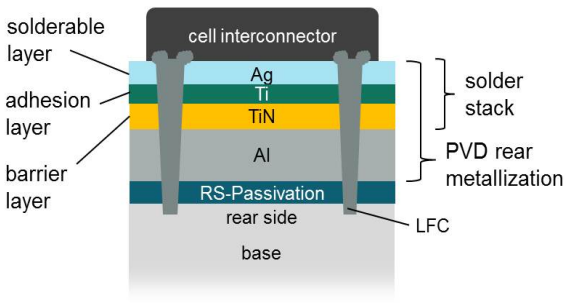

Figure 1: Cross-section of PVD rear metallization scheme for LFC-PERC solar cell (rear side facing up, not to scale)

3 THERMAL STABILITY

3.1 Sample preparation

The proposed metallization concept is investigated in respect of thermal stability by the experimental approach shown in Fig. 2.

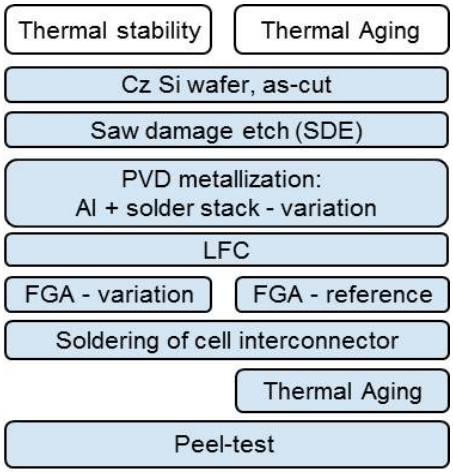

Figure 2: Process sequence for investigation of thermal stability and thermal aging

On damage-etched Czochralski-grown Si wafers the PVD metallization stack is deposited in one process sequence using an industrial prototype PVD machine with evaporation The PVD metallization in each case consists of a 2 µm thick evaporated Al layer and a solder stack, which is varied according to Table I. Then LFC are applied, followed by a forming gas anneal at varying temperatures (see Table I). It is then attempted to solder a cell interconnector onto the metallization by means of a common manual soldering process using conventional solder and interconnectors. If the solder attempt is successful, the quality of the solder joint is evaluated in a 90°-peel test after standard DIN EN 50461, which is passed when a 2 mm wide cell interconnector is peeled off with forces of at least 2 N.

3.2 Solderability and adhesion results

After the samples with evaporated Al and a first solder stack, consisting of 100 nm TiN, 20 nm Ti and 150 nm Ag (see solder stack A in Table I), are annealed for 3:40 min at 350°C, which is the TOPAS PERC reference annealing step, it is still possible to solder a standard cell-interconnector onto the metallization. As can be seen from the exemplary peel-test diagram in Fig. 3, it passes a subsequent peel-test with sufficiently high forces. This is indicated in Table I by a green checkmark.

Therefore the metallization shows a sufficient thermal stability for being applied to the TOPAS PERC design. To investigate the limit of thermal stability of the solder stack and its applicability to cell designs that might benefit from a stronger annealing step, some samples are also annealed at higher temperatures. The results of solder attempt and peel-test show that the metallization also withstands an annealing of 3:40 min at 400°C, but it fails at stronger annealing conditions of 18 min at 425°C. This is indicated by a red cross in Table I.

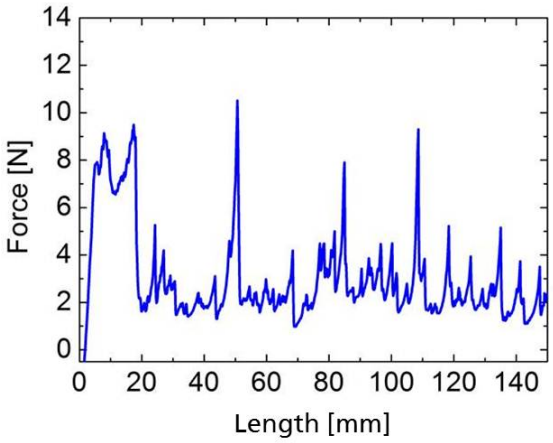

Figure 3: Peel-test diagram: A 2 mm wide cell-interconnector, manually soldered onto a sample with solder stack A and annealed for 3:40 at 350°C, is subsequently peeled with sufficiently high forces.

Table I: Summary of results. A green checkmark for solderability indicates that after the listed annealing conditions a soldering attempt is successful and the peel-test is passed, whereas the red cross indicates that at least one of these two fails. The same symbols in respect of thermal aging indicate if the peel-test after aging is passed.

Solder stack	**Label**	**A**	**B**	**C**	**D**	**E**	**F**
	Specifications	150 nm Ag 20 nm Ti 100 nm TiN	100 nm Ag 20 nm Ti 100 nm TiN	50 nm Ag 20 nm Ti 100 nm TiN	150 nm Ag 20 nm Ti 100 nm TiN_{mod}	25 nm Ag 20 nm Ti 100 nm TiN_{mod}	25 nm Ag 100 nm NiV 100nm TiN_{mod}
Solderability after FGA	**350°C, 3:40 min (reference)**	✓	✓	✓	✓	✓	✓
	400°C, 3:40 min	✓	✗	✗	✓	✗	✓
	425°C, 18 min	✗	✗	✗	✓	✗	*
	450°C, 18 min	✗	✗	✗	✗	✗	✗
Thermal aging	Adhesion after 85 h at 130°C	✓	✓	✗	✓	✗	✓
Silver consumption	Amount Ag on rear side of 156 mm cell	36 mg	24 mg	12 mg	36 mg	6 mg	6 mg
Cost	Cost for consumables [€ct/wafer]	6.0	4.3	2.5	6.0	1.6	3.0

* not tested

Regarding material consumption and cost-efficiency it is desirable to reduce the amount of Ag which is needed for the solder stack. The proposed stack with an Ag layer of 150 nm thickness corresponds to 36 mg of Ag on a 156 mm large cell rear side. It is attempted to reduce the amount of Ag consumption by repeating the investigation with solder stacks (labelled B and C in Table I) with reduced Ag layer thicknesses of 100 nm and 50 nm. As can be seen in Table I the stack does not withstand elevated annealing steps, but it remains solderable after the reference annealing step at 350°C for 3:40 min. Therefore, in respect to the PERC concept, the Ag amount on the rear of a cell can be reduced to 12 mg. A further reduction of the Ag layer thickness to 25 nm leads to a reduced adhesion which fails the peel-test standard.

The thermal stability of the solder stack can be enhanced by using a modified TiN barrier layer (TiN_{mod}). The modified solder stack of 100 nm TiN_{mod}, 20 nm Ti and 150 nm Ag (labelled D in Table I) is investigated as before and shows a significantly improved thermal stability. The metallization remains solderable and passes the peel-test after a strong annealing step of 18 min at 425°C, which is considered to be sufficient for most silicon solar cell concepts which might use PVD Al metallization. Again it is attempted to reduce the amount of Ag in the solder stack. A stack using a just 25 nm thick Ag layer in combination with 60 nm TiN_{mod} is found to be solderable and sufficiently adhering after the reference anneal at 350°C for 3:40 min, which corresponds to an Ag amount of only 6 mg on the rear of a PERC cell.

A second possibility for reducing the Ag layer thickness can be effectuated by using NiV as main solderable layer complemented by just a thin Ag layer to protect the NiV layer from oxidation, similar to [6]. A stack, labelled F in Table I, of 100 nm TiN_{mod}, 100 nm NiV and 25 nm Ag is investigated as before and shows solderability and good adhesion after annealing at 350°C and 400°C while using only 6 mg Ag. A Ti adhesion layer is not needed in this combination of materials.

In summary, due to the TiN barrier layer all the presented stacks A-F remain stable during PERC reference annealing conditions (350°C for 3:40 min). The amount of silver on the sample needed for enabling rear solderability is reduced to 6 mg per cell. If different solar cell concepts with stronger annealing conditions are pursued, 100 nm of the modified TiN_{mod} as used in stack D should be sufficient to guarantee thermal stability and solderability for most practical demands. A reduction of Ag thickness for these stacks is currently investigated.

4 ACCELERATED AGING

To estimate long-term stability of solder joints that base on the presented solder stacks, an accelerated aging test as described in [12] is performed.

Test samples are prepared after the process flow for thermal aging in Fig. 2, using the different solder stacks A-F and annealing conditions of 350°C for 3:40 min. Then, cell-interconnectors are soldered onto the metallization and the samples are isothermally aged in nitrogen atmosphere for 85 h at 130°C which corresponds to about 20 years at 20°C in terms of thermal activation. Subsequently, the quality of the aged solder-joints is characterized by peel-testing the cell-interconnectors as before. Though evidently the accelerated aging procedure does not replace the IEC standards for evaluating long-term stability of solar cells and modules, the accelerated aging test provides an easily applicable means to compare the quality of solder-joints based on the different stacks with respect to aging. The results of the peel-tests are depicted in Table I and it can be seen that the solder-joints which base on the solder stacks C and E, which possess the thinnest Ag layers, do not pass the test whereas the solder-joints on the other stacks withstand the thermal aging procedure. However, stack F with an only 25 nm thick Ag layer passes the test which we attribute to the presence of the 100 nm thick NiV layer underneath the Ag layer.

5 COST CALCULATION

A solderable PVD metallization has the potential of being a cost-efficient alternative to other technologies as e.g. screen-printing, since material consumption is significantly lower. A cost of ownership calculation is done based on the SCost tool [13].

The cost for consumables of a PVD rear metallization with the presented solder stacks are depicted in Table I, e.g. cost of consumables for a PVD metallization consisting of 2 µm Al, 100 nm TiN_{mod}, 100 nm NiV and 25 nm Ag reach 3.0 €ct/wafer, when it is considered that about 60% of the target material is actually deposited on the wafer. Stack E causes costs of only 1.6 €ct/wafer for consumables. These costs are especially sensitive to the Ag price which is assumed to be 529 €/kg (silver fixing on 17/09/2013). When all cost for equipment, labour, parts, utilities and consumables are considered, process cost of a PVD rear metallization largely depend on the cost of the PVD machine. With conservative assumptions (7.9 M€ invest for a PVD machine with 120 MWp/a throughput, 5 years depreciation period) a PVD metallization can be realized at cost of 13.5 €ct/wafer. However, for the future we expect a significant cost saving potential due to economies of scale which makes PVD metallization distinctly cost-efficient compared to screen-printing.

6 SUMMARY

A solderable Al based PVD metallization scheme, which consists of evaporated Al and a stable solder stack, is introduced and investigated in this work.

Different versions of the solder stack, which all consist of a TiN barrier layer and a solderable top layer, are investigated on test samples. We thus prove the metallization scheme to be temperature-stable and remain solderable during a typical final annealing step for LFC-PERC solar cells. The stability of the metallization can be further enhanced by modifying the TiN barrier layer. Thus, solderability is sustained after an annealing step for 18 min at 425°C, which is considered sufficient for most solar cell concepts. At the same time we reduce the amount of Ag, which is needed for achieving a solderable, annealing stable metallization, to only 6 mg/wafer (156mm size). An accelerated aging test which corresponds to thermal activation during 20 years at 20°C, is passed by four of the six investigated stacks. A cost calculation is done and we consider the developed metallization scheme as potentially cost-efficient.

To conclude, by complementing an evaporated Al layer with a stable solder stack, we develop an industrially feasible, temperature stable and solderable Al based PVD metallization scheme which is suitable not just for PERC silicon solar cells.

7 ACKNOWLEDGEMENT

The authors would like to thank all colleagues at Fraunhofer ISE, especially Dirk Eberlein and Peter Schmitt for their support.

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